Fig 1

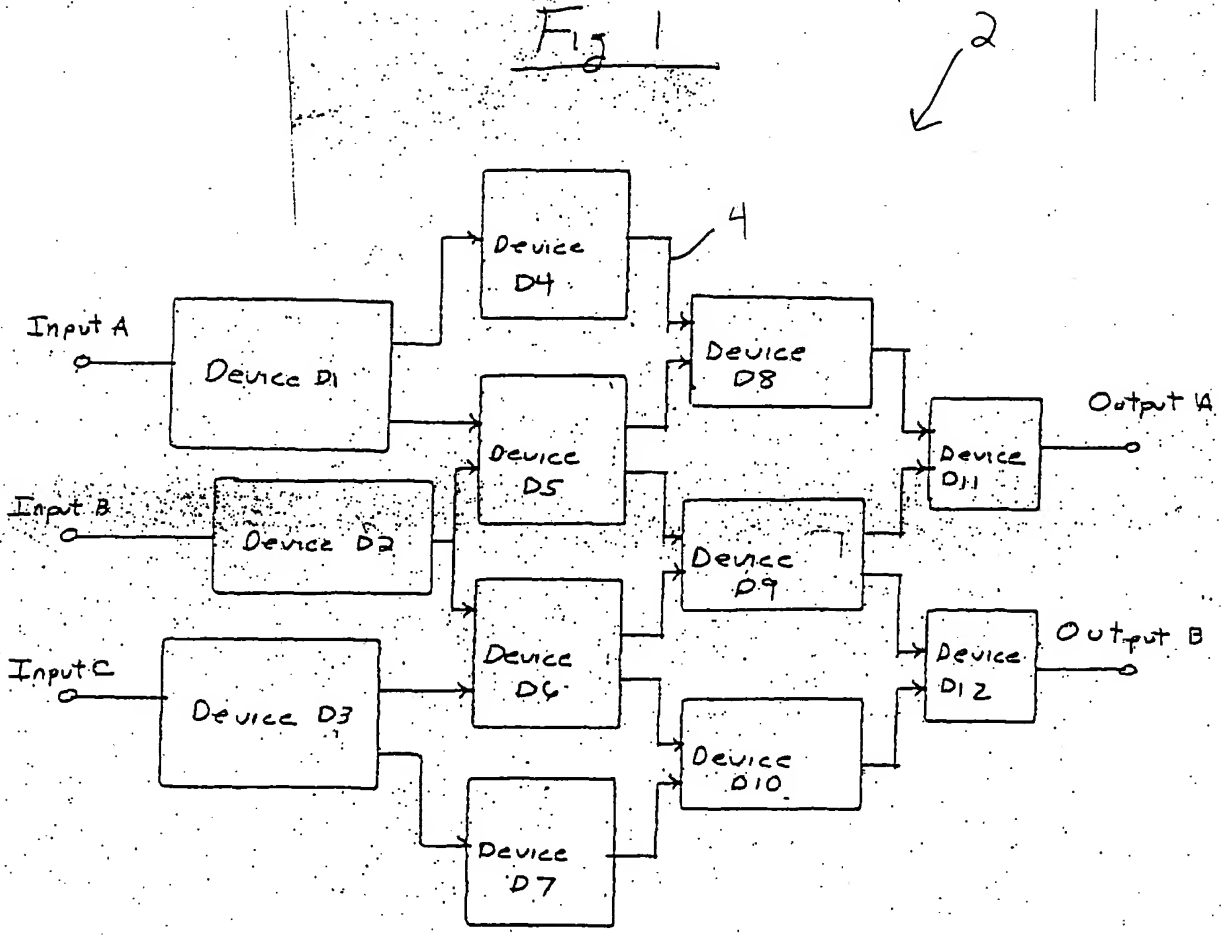
2
4
Input A
Input B
Input C
Device D1
Device D2
Device D3
Device D4
Device D5
Device D6
Device D7
Device D8
Device D9
Device D10
Device D11
Device D12
Output A
Output B

Fig 2

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Device(s) 8			Synthesized Performance Specification(s)*
Device #	Device Variable(s)	Device Constants(s)	
D1 (Input Transistor)	Length & width	Area	Gain (G) 6
D2 (Input Transistor)	"	"	
D3 (Input Transistor)	"	"	Slew Rate (SR)
D4 (Resistor)	Resistance	Length & width	
D5 (Capacitor)	Capacitance	"	Unity Gain Freq (UGF)
D6 (Resistor)		"	
D7 (Capacitor)		"	Input offset (IO)
D8 (Resistor)	Resistance		Phase Margin (PM)
D9 (Resistor)	"		Settling Time (ST)
D10 (Resistor)	"		Power (Useage) (P)
D11 (Output Transistor)	Length & width	Area	Estimated Total Area (ETA)
D12 (Output Transistor)	"	Area	

* Performance Specifications to be compared to circuit Performances determined by a circuit Synthesizer

Fig 3

Synthesized Design Population

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Design Point	Circuit Topology	Performance(s)	Original Cost	Domination Cost	Tradeoff Cost	Relative Efficiency
DP1	T_{DP1}	G_{P-DP1}, SR_{P-DP1} ⋮ ETA_{P-DP1}	OC_{DP1}	DC_{DP1}	TC_{DP1}	RE_{DP1}
DP5	T_{DP5}	G_{P-DP5} SR_{P-DP5} ⋮ ETA_{P-DP5}	OC_{DP5}	DC_{DP5}	TC_{DP5}	RE_{DP5}
DP7	T_{DP7}	G_{P-DP7} SR_{P-DP7} ⋮ ETA_{P-DP7}	OC_{DP7}	DC_{DP7}	TC_{DP7}	RE_{DP7}
DPX	T_{DPX}	G_{P-DPX} SR_{P-DPX} ⋮ TA_{P-DPX}	OC_{DPX}	DC_{DPX}	TC_{DPX}	RE_{DPX}

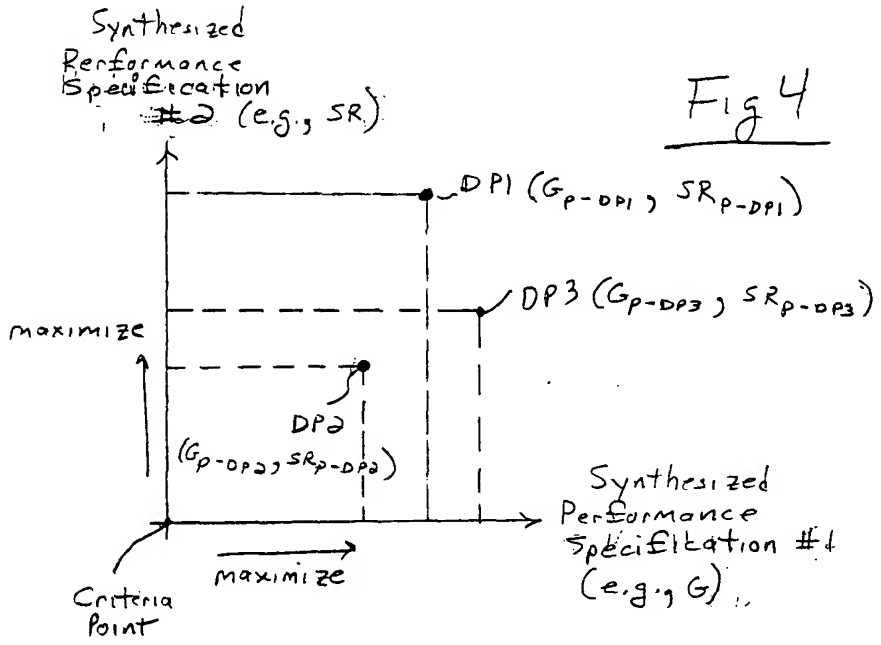

Synthesized Performance Specification #2 (e.g., SR)
DP1 (G_{p-DP1}, SR_{p-DP1})
DP3 (G_{p-DP3}, SR_{p-DP3})
maximize
DP2
(G_{p-DP2}, SR_{p-DP2})
Synthesized Performance Specification #1 (e.g., G)
maximize
Criteria Point

Fig 4

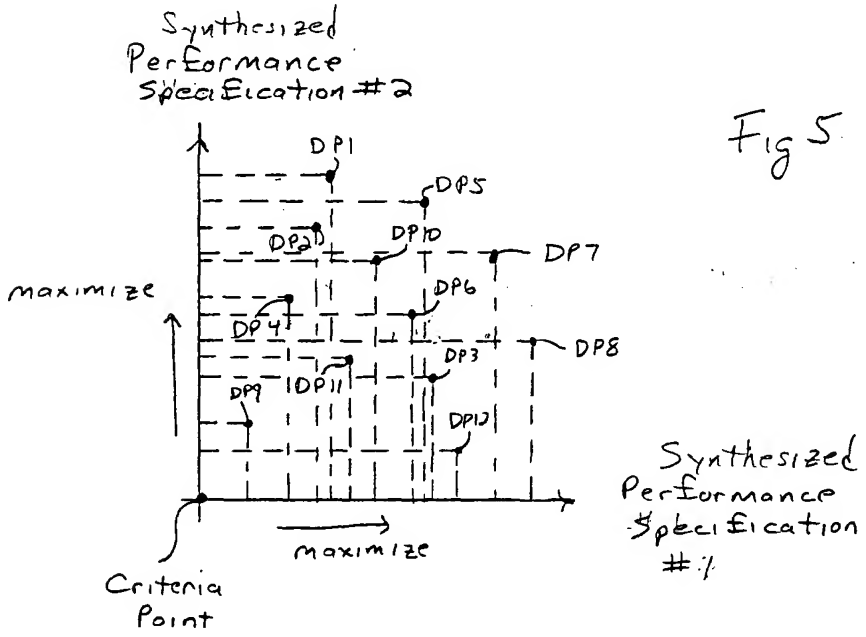

Synthesized Performance Specification #2
DP1
DP5
DP2
DP10
DP7
maximize
DP6
DP4
DP3
DP8
DP11
DP9
DP12
Synthesized Performance Specification #1
maximize
Criteria Point

Fig 5

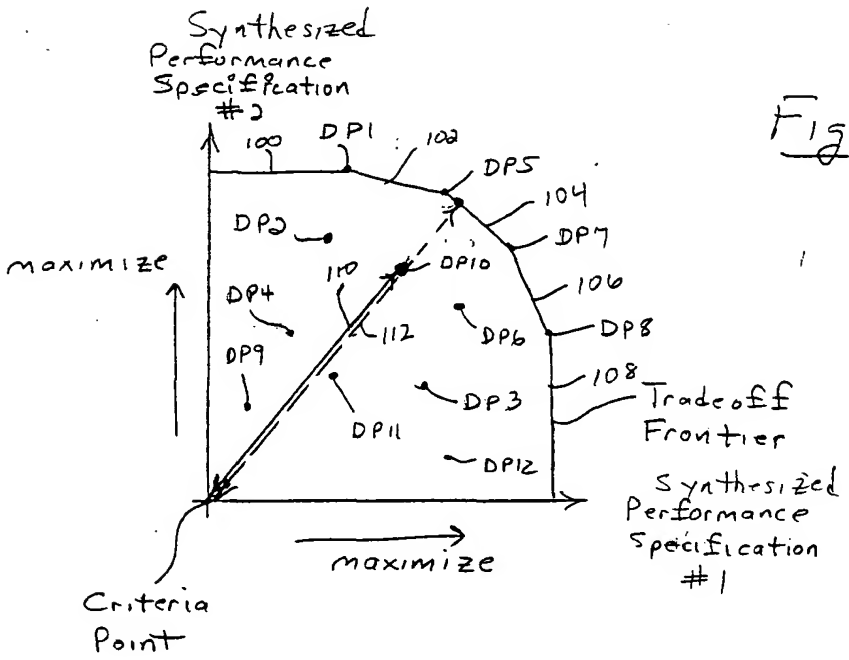

Synthesized Performance Specification #2
maximize
DP1
DP2
DP3
DP4
DP5
DP6
DP7
DP8
DP9
DP10
DP11
DP12
100
102
104
106
108
110
112
Tradeoff Frontier
Synthesized Performance Specification #1
maximize
Criteria Point

Fig 6

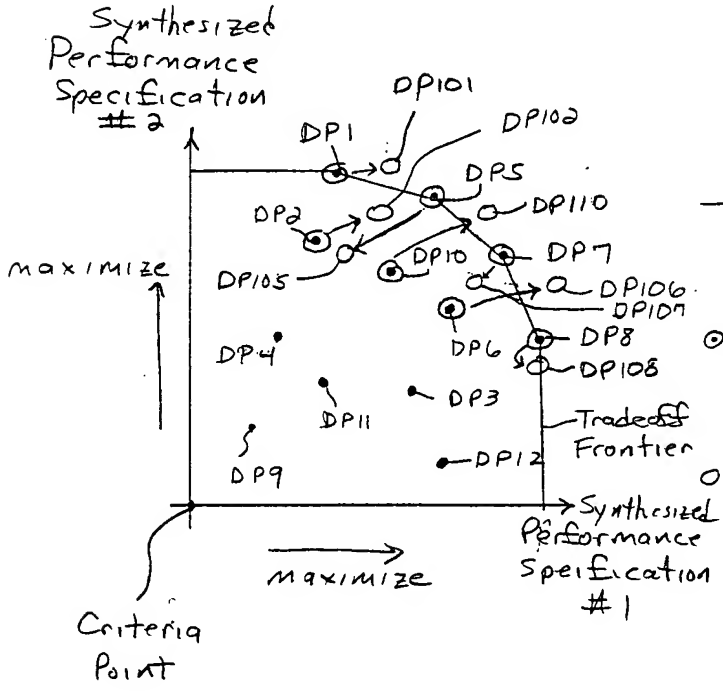
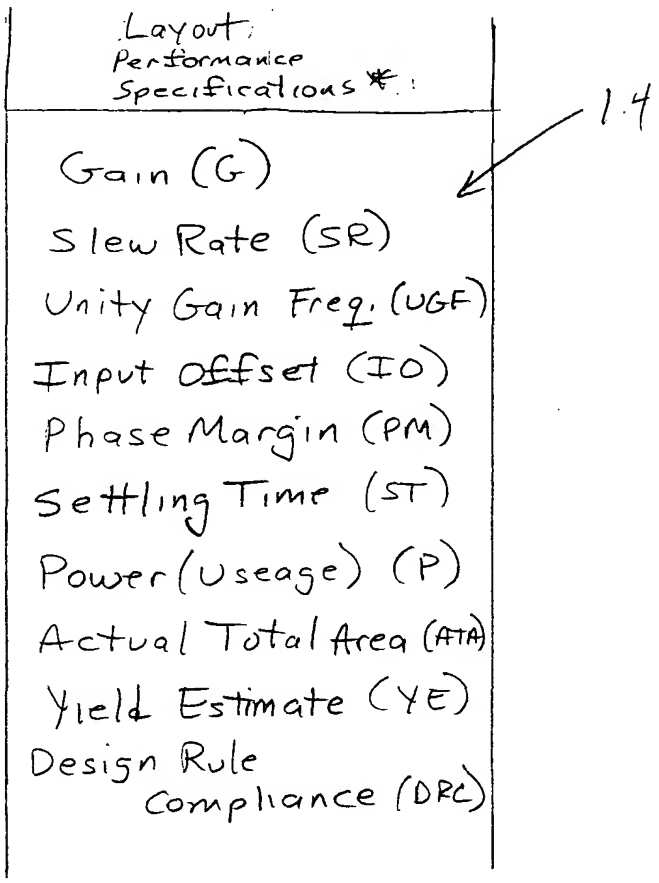


Fig 7

⊙ = Design Points with Lowest Tradeoff Cost

○ = New Design Points Generated from Design Points with Lowest Tradeoff Costs

Fig 8



* Performance Specifications to be compared to Circuit Performances determined by a circuit simulator.

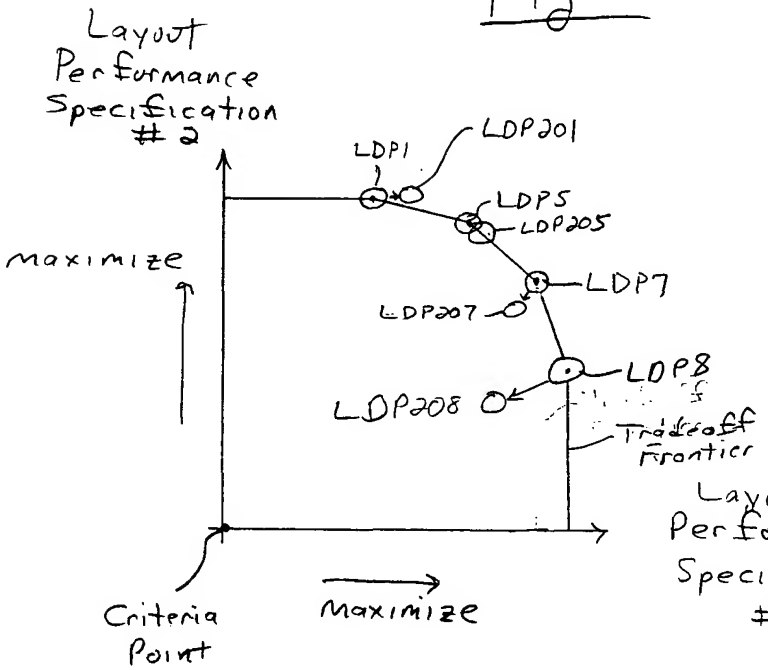
Fig 9

16

Layout Design Population

Layout Design Point	Circuit Layout	Performance(s)	Original Cost	Domination Cost	Tradeoff Cost	Relative Efficiency
LDP1	L_{LDP1}	G_{P-LDP1} SR_{P-LDP1} ⋮ DRC_{P-LDP1}	OC_{LDP1}	DC_{LDP1}	TC_{LDP1}	RE_{LDP1}
LDP5	L_{LDP5}	G_{P-LDP5} SR_{P-LDP5} ⋮ DRC_{P-LDP5}	OC_{LDP5}	DC_{LDP5}	TC_{LDP5}	RE_{LDP5}
LDP7	L_{LDP7}	G_{P-LDP7} SR_{P-LDP7} ⋮ DRC_{P-LDP7}	OC_{LDP7}	DC_{LDP7}	TC_{LDP7}	RE_{LDP7}
LDPX	L_{LDPX}	G_{P-LDPX} SR_{P-LDPX} ⋮ DRC_{P-LDPX}	OC_{LPDX}	DC_{LDPX}	TC_{LDPX}	RE_{LDPX}

Fig 10



⊙ = Layout Design Point Generated from Design Points with Lowest Tradeoff Cost

○ = New Layout Design Point Generated from Layout Design Points Generated from Design Points with Lowest Tradeoff Costs